Minimizing Ringing and Crosstalk

by Glen Dash
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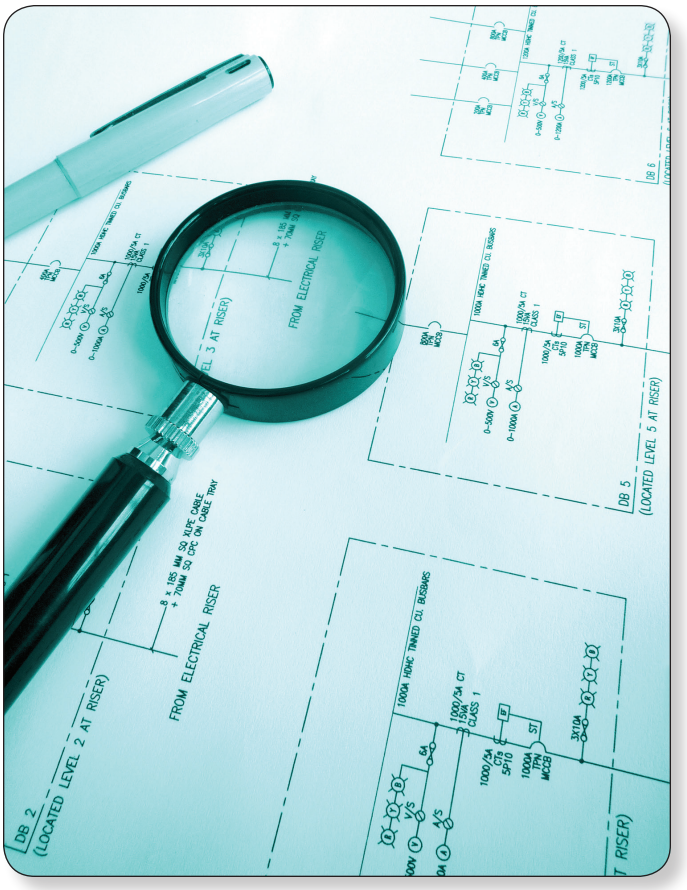

When viewed on a schematic, a wire is just a wire. However, when risetimes shrink to a few nanoseconds or less, wires become radiators. To conduct signals with good fidelity at these speeds, wires should be paired with their returns, forming transmission lines.

A wire over a return plane forms a kind of transmission line known as a microstrip. A trace between two planes forms a stripline. Both must be well designed to avoid ringing and crosstalk. To avoid ringing, impedances must be matched. To avoid crosstalk, spacings must be selected with care. Even in an age of automated routing checks and signal integrity software, controlling ringing and crosstalk is part science, part art.

Transmission line effects become significant when the trace is long enough, or the risetime is fast enough, for propagation times to be significant. One oft-cited rule of thumb states the following [4]:

Maximum Length for a Microstrip = $9 \times t_r$

Maximum Length for a Stripline = $7 \times t_r$

Where:

Maximum Length = Maximum length of the trace in centimeters before transmission line effects must be considered.

t_r = Risetime in nanoseconds

For a Microstrip:	$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98H}{.8W + T}\right)$ $C_0 = \frac{.67(\varepsilon_r + 1.41)}{\ln\left[\frac{5.98H}{.8W + T}\right]}$
For an Embedded Microstrip:	$Z_0 = \frac{60}{\varepsilon_{r'}} \ln\left[\frac{5.98H}{.8W + T}\right]$ Where: $r' = r\left(1 - e^{\left(\frac{-1.55H1}{H}\right)}\right)$ $C_0 = \frac{1.41r'}{\ln\left[\frac{5.98H}{.8W + T}\right]}$
For a Stripline:	$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{1.9(2H + T)}{.8W + T}\right)$ $C_0 = \frac{1.41\varepsilon_r}{\ln\left[\frac{3.81H}{.8W + T}\right]}$

Notes: Z_0 is in ohms, C_0 is in pf/inch. See Figure 2 for dimensions.

Table 1: Characteristic Impedances of Microstrips and Striplines [2]

For a risetime of .9 nsec, this translates to 8.1 cm for microstrips and 6.3 cm for striplines. Since it is rarely possible to keep all traces so short, impedances need to be matched to control ringing.

One of these four impedance-matching methods are generally applied:

1. Series termination in "standard" or "star" topography,
2. DC parallel termination,
3. AC parallel termination, or
4. Diode termination.

Of these, series termination is the clear favorite among digital hardware designers. Its advantage is in its simplicity. Its chief disadvantage is in its implementation. Accurately calculating a real-world transmission line's impedance can be tricky.

DC parallel termination is a modern name for the traditional impedance matching topology used by communications engineers. Conceptually, it is the most straight-forward. A load impedance is chosen to match the impedance of the transmission line. For logic circuits, however, DC parallel termination has significant disadvantages and is rarely used. It lowers the impedance as seen from the driver and increases power dissipation.

AC parallel termination solves some of these problems. Its chief disadvantage is in its need for a capacitor at the load end.

Diode termination works as follows. Since the impedance of a diode changes dynamically with current, it is possible to dynamically match the impedance of a transmission line. In practice, however, diode termination can be difficult to implement. Very fast diodes are required and nonlinear effects can be generated.

For topologies other than diode termination, proper implementation requires that the transmission line impedance be known. Handbook formulas such as those shown in the table provide insight, but in practice are often inadequate. For example, author Douglas Brooks points out that the formula for an embedded microstrip shown in Table 1 can only be considered reliable if the same dielectric material is used both

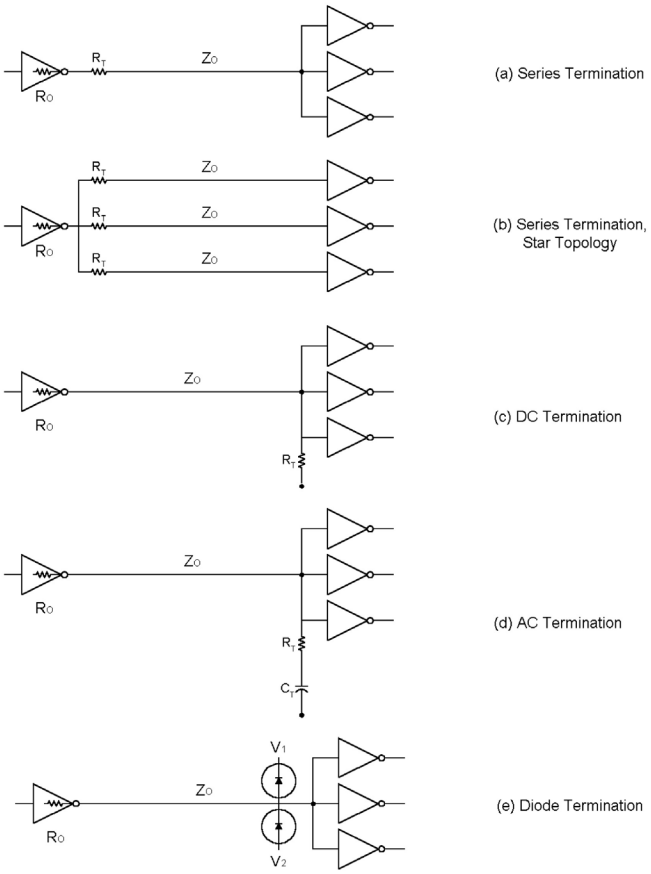

Figure 1: Of the topologies available to designers, the series termination is a clear favorite among digital designers. A "star" topology can be used to drive widely spaced loads.

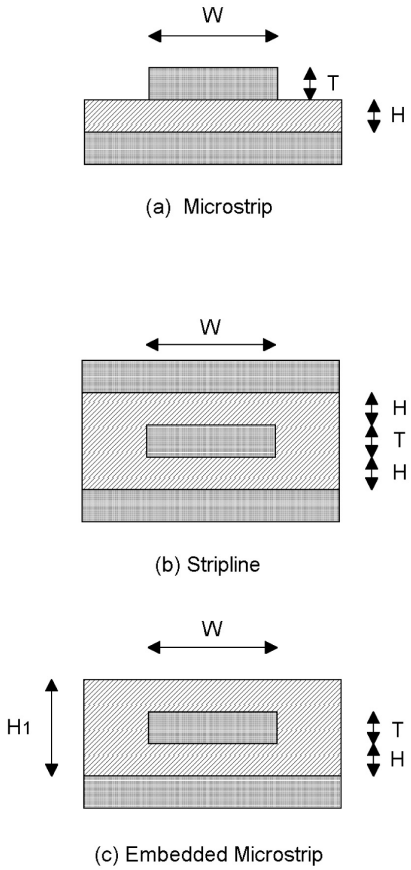

Figure 2: Transmission line types commonly used in PCB designs. For characteristic impedance and capacitance per unit length, see Table 1. [2]

above and below the signal trace, and if the dielectric above the trace is more than 4 mils thick. Similar limitations apply to the other formulas.

Fortunately, software is widely available that takes such matters into consideration. For freeware versions, check out Polar Instrument's site at www.polarinstruments.com, designer Barry Olney's site at www.icd.com.au, or UltraCad Design's site at www.ultracad.com.

Once the characteristic impedance has been established, the topology best suited for implementing series termination depends on (1) the number of loads driven and (2) their physical proximity. When a single driver is driving a single load or a group of loads placed in close proximity the matching resistor (R) should be equal to the characteristic impedance (Z0) minus the resistance of the driver (RO). (Typical trace impedances are 60 to 100 ohms, and driver impedances, 2 to 20 ohms.) Where loads are widely separated, a scheme known as "star routing" can be used which places a separate resistor in each line (Figure 1). Note that the impedance as seen by the driver is equal to impedance of all the connections in parallel. In order to prevent excessive loading, the parallel impedance of all these traces must be much greater than the output impedance of the driver. Drive limitations can crop up even when relatively few branches are used, and well before the device's fan out is reached.

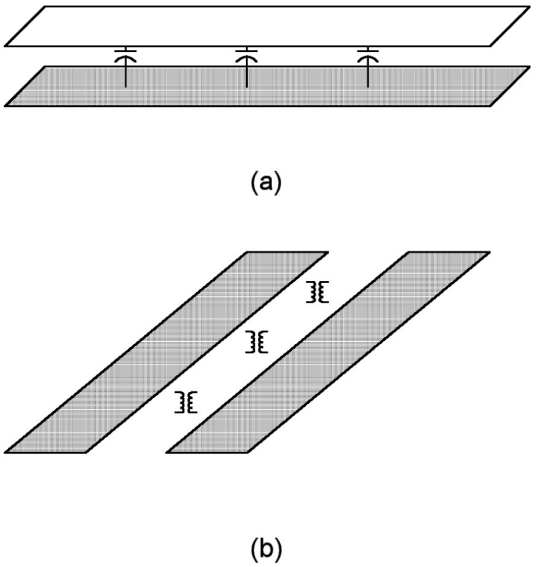

Figure 3: Two traces placed one on top of the other as in (a) primarily couple capacitively. Traces placed side by side as in (b) primarily couple inductively.

Predicting exactly what happens to a transmitted pulse when series termination is used can be complex. Motorola provides a useful reference [6]. Since series termination matches the source end of the line, pulses sent down the line are reflected and absorbed at the source end. Because of that, a type of distortion known as "stair casing" is inherent in the design and must be kept within acceptable limits.

Crosstalk is a primarily a near field phenomenon. Depending on the relative placement of "source" and "victim" traces, it can be analyzed primarily as an electric field problem (voltage driven, capacitive in nature) or a magnetic field problem (current driven, inductive in nature). As a general rule, traces placed one over another will primarily exhibit capacitive coupling, whereas two traces placed side by side primarily couple magnetically . We will refer to the two as examples of "capacitive" and "inductive" crosstalk respectively.

Capacitive crosstalk is the easiest grasp. The two traces form a capacitor. Minimizing problems means minimizing the size of the capacitor. Therefore, high-speed traces on adjacent layers of a printed circuit board should not be run one on top of the other. Such traces, if crossed at all, should cross at right angles, limiting the area of the capacitor formed.

Two traces placed side-by-side as in Figure 3(b) form a kind of transformer. The magnetic field produced by one couples to the other. The coupled signals travel down the victim line both toward the load and backwards toward the source. In practice, it is the "backward crosstalk" that generally proves to be the most troublesome.

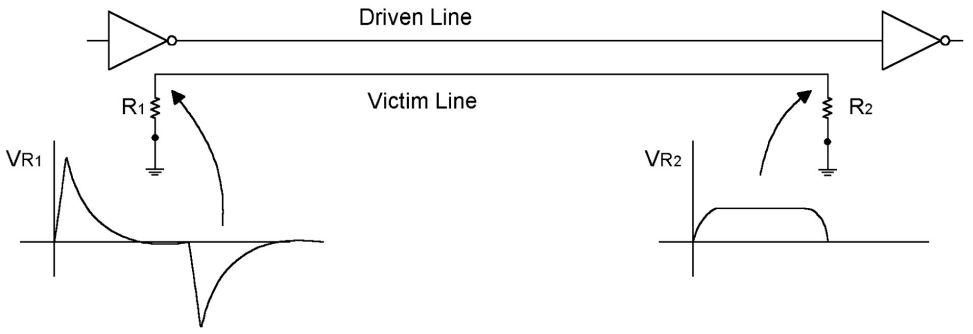

Figure 4: A driven trace placed side by side with a victim trace produces both "forward" and "backward" moving signals on the victim line. Of these, the backward moving signal is generally considered the most troublesome.

The degree of inductive crosstalk experienced is largely due to three factors: (1) the common length of the two traces, (2) the edge-to-edge separation between traces, and (3) the distance between the traces and the nearest power plane.

Obviously, the most straightforward method of reducing inductive crosstalk is to shorten the common length among any two traces. But this solution is often not as practical as it at first might seem. To see why this is so, think of the two traces as two windings on a transformer. The coupling between the driven and victim line is analogous to the coupling coefficient of a transformer. As a practical matter, this coupling coefficient gets near unity for closely spaced, parallel traces even if they run parallel for only a few inches. Once the coupling is at unity, making the traces longer will not hurt much. Conversely, making them slightly shorter will not help much either. The common length at which coupling approaches unity is known as the "critical length" or the "saturation point."

Because the critical point is reached so readily, it is often more practical to focus on two other factors which affect inductive crosstalk, the spacing between the traces and their height above the nearest power plane. We will want to keep coupling below a permissible level, say 5% for TTL to TTL coupling. Figure 6 can be used as a guide. For example, if the height above the nearest ground plane is 5 mils, use a trace-to-trace separation of approximately 15 mils. If the height is 10 mils, the trace-to-trace separation will have to be closer to 30 mils.

The amount of coupling allowed should be tailored to the technology used. Five percent is usually sufficient when both the victim line and the driven line are MOS, or both are TTL. In the case of mixed logic, such as when a MOS line runs parallel to an ECL or PCI bus, less coupling should be allowed. [3]. ■

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Glen Dash is the author of numerous papers on electromagnetics. He was educated at MIT and was the founder of several companies dedicated to helping companies achieve regulatory compliance. Currently he operates the Glen Dash Foundation which uses ground penetrating radar to map archaeological sites, principally in Egypt.

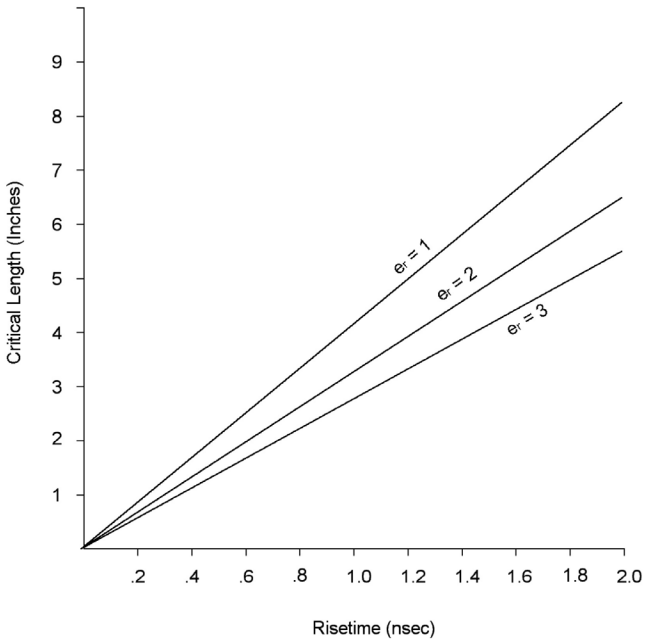

Figure 5: The "critical length" for two closely spaced parallel traces is the common length at which the coupling coefficient is close to one. Beyond this point, making the common length longer will not make things worse, nor will shortening the traces slightly make things much better. Therefore, it is often better to concentrate on the trace-to-trace spacing and the distance above the nearest power plane as illustrated in Figure 6. [3]

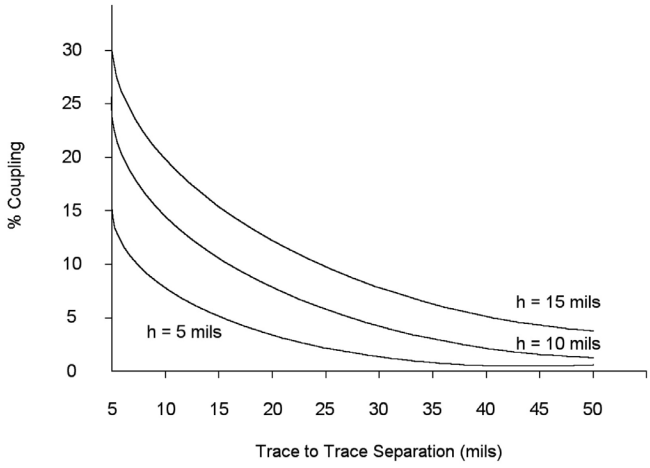

Figure 6: Once the height above the nearest power plane is known, trace to trace spacing can be selected to reduce coupling to an acceptable level. [3]